What is claimed is:

1. A multichip module including a module substrate having plural wiring layers, many external connecting electrodes formed on one face of said module substrate, and a mounting pad for mounting plural semiconductor integrated circuit chips formed on the other face of said module substrate;

wherein said mounting pad is separated into an area of the mounting pad of the plural semiconductor integrated circuit chips able to be relatively operated at high speed, and an area of the mounting pad of the plural semiconductor integrated circuit chips operated at relatively low speed; and

the external connecting electrodes corresponding to an address output and a data input-output are arranged on a rear face of said area for mounting the plural semiconductor integrated circuit chips operated at relatively low speed.

2. A multichip module according to claim 1, wherein relatively many external connecting electrodes allocated to the supply of a power voltage and a ground voltage are arranged on a rear face of said area for mounting the plural semiconductor integrated circuit chips operated at relatively high speed.

3. A multichip module including a module substrate having plural wiring layers, many external connecting electrodes formed on one face of said module substrate, and a data

processor chip, memory chips and buffer circuits connected to said wiring layers on the other face of said module substrate;

wherein the data processor chip is arranged approximately at the center of said module substrate, and the plural memory chips are arranged on one side and the plural buffer circuits are arranged on the other side in parallel with each other through said data processor chip.

4. A semiconductor module including a module substrate having plural wiring layers, many external connecting electrodes formed on one face of said module substrate, a mounting pad formed on the other face of said module substrate, and a data processor chip, a memory chip and a buffer circuit arranged through said mounting pad;

wherein the external connecting electrodes allocated for an address and data are arranged on the rear face of an area for mounting said buffer circuit.

5. A multichip module including a module substrate having plural wiring layers, many external connecting electrodes formed on one face of said module substrate, a mounting pad formed on the other face of said module substrate, and a data processor chip, a memory chip and a buffer circuit arranged through said mounting pad;

wherein relatively many external connecting electrodes allocated to supply a power voltage and a ground voltage are arranged on the rear face of an area for mounting said memory

chip.

6. A multichip module including a module substrate having plural wiring layers, many external connecting electrodes formed on one face of said module substrate, a mounting pad formed on the other face of said module substrate, and plural kinds of semiconductor integrated circuit chips mounted through said mounting pad;

wherein the external connecting electrodes for operating power allocated to supply a power voltage and a ground voltage are coarsely and closely arranged on the module substrate, and are closely arranged on rear faces of the semiconductor integrated circuit chips having larger power consumption.

7. A semiconductor module in which plural external connecting electrodes are arranged on one face of a module substrate and a mounting pattern is formed on the other face of the module substrate;

said mounting pattern includes a grouped pattern able to arrange semiconductor integrated circuit chips approximately having an equal height size in one line and mount these semiconductor integrated circuit chips every group of the semiconductor integrated circuit chips; and

the mounting pattern and a bump electrode of the semiconductor integrated circuit chip are electroconductively connected to each other through an anisotropic

electroconductive film stuck every said grouped pattern.

8. An electronic circuit including a first semiconductor device and a second semiconductor device able to be operated at high speed in comparison with said first semiconductor device wherein the first and second semiconductor devices are mounted to a bus of a wiring substrate in a common connecting state;

wherein said second semiconductor device has a data processor chip and a memory chip commonly connected to said bus through an external connecting electrode in a multilayer wiring substrate, and includes a buffer circuit in a wiring path from said data processor chip and the memory chip to said external connecting electrode;

said buffer circuit interrupts an input from said bus in access of the memory chip using said data processor chip; and

the external connecting electrode allocated for an address and data is arranged on the rear face of an area for mounting said buffer circuit.

9. An electronic circuit according to claim 8, wherein said buffer circuit is an address output buffer, a control signal output buffer and a data input/output buffer respectively inserted into said wiring path; and

said data input/output buffer is controlled to a high impedance state in response to an access command of the memory

chip given by said data processor chip.

10. An electronic circuit according to claim 9, wherein said buffer circuit is an address input/output buffer, a control signal input/output buffer and a data input/output buffer respectively inserted into said wiring path, and

said address input/output buffer, the control signal input/output buffer and the data input/output buffer are controlled to the high impedance state in response to the access command of the memory chip given by said data processor chip.

11. An electronic circuit according to claim 8, wherein relatively many external connecting electrodes allocated to supply a power voltage and a ground voltage are arranged on the rear face of an area for mounting said memory chip.